Applicants : Kuo et al.
Serial No. : 10751,263
Filed : December 30, 2003
Page : 2 of 14

Attorney's Docket No.: Intel-010PUS
Intel Docket No.: P17937

AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method comprising:

assigning a first memory to a first memory channel;

assigning a second memory to a second memory channel; the first memory being equal in memory size to the second memory;

assigning a third memory to a third memory channel; the third memory comprising a first memory portion being equal in memory size to the first memory and comprising a second memory portion;

interleaving the first memory, the second memory and the first memory portion of the third memory in a three-way interleaving;

~~allocating memory non-uniformly between a plurality of memory channels associated with a network processor;~~

determining a selected memory channel from the first memory channel, the second memory channel and the third memory channel ~~said plurality of memory channels~~ for a program address; and

Applicants : Kuo et al.
Serial No. : 10751,263
Filed : December 30, 2003
Page : 3 of 14

Attorney's Docket No.: Intel-010PUS
Intel Docket No.: P17937

mapping said program address to a physical address within said selected memory channel.

2. (Cancelled)

3. (Original) The method of claim 1 wherein said determining a selected memory channel comprises:

determining whether the program address accesses an interleaved portion of memory and when said program memory address does access an interleaved portion of memory then performing an operation on said program address to obtain a memory channel number and when said program memory address does not access an interleaved portion of memory then selecting the memory channel containing non-interleaved memory.

4. (Original) The method of claim 1 wherein said mapping said program address to a physical address comprises:

determining whether the program address accesses an interleaved portion of memory and when said program memory address does access the interleaved portion of memory then performing address interleaving of said program address and when said program memory address does not access the interleaved portion of memory then subtracting a predetermined value from said program address to obtain a physical address in the selected memory channel.

Applicants: Kuo et al.
Serial No. : 10751,263
Filed : December 30, 2003
Page : 4 of 14

Attorney's Docket No.: Intel-010PUS
Intel Docket No.: P17937

5. (Currently Amended) The method of claim [[2]] 1 wherein said interleaving comprises:

determining the number of consecutive bits of a predetermined portion of the program address bits that are ones;

right shifting program address bits by a predetermined number of bits to obtain a shifted address;

adding a predetermined offset value to the shifted address to obtain an interim physical address; and

appending a predetermined number of program address bits to said interim physical address to obtain a physical address within said selected memory channel.

6. (Cancelled)

7. (Cancelled)

8. (Original) The method of claim 3 wherein said determining whether the program address accesses an interleaved portion of memory comprises determining whether the program address accesses a lower three/fourths of memory.

9. (Original) The method of claim 3 wherein said performing an operation on said program address comprises performing summing modulo three arithmetic on at least a portion of

said program address to obtain a remainder, said remainder comprising the memory channel

number

10. (Currently Amended) A system comprising

a network processor; and

a plurality of memory channels in communication with said network processor, <u>the</u>

<u>plurality of memory channels comprising a first memory channel access a first memory, a second</u>

<u>memory channel accessing a second memory and a third memory channel accessing a third</u>

<u>memory, the first memory being equal in memory size to the second memory, the third memory</u>

<u>comprising a first memory portion being equal in memory size to the first memory and</u>

<u>comprising a second memory portion,</u>

wherein <u>the first memory, the second memory and the first memory portion of the third</u>

<u>memory are configured to be interleaved in a three-way interleaving;</u> ~~at least one of said memory~~

~~channels has more memory than another of said memory channels~~.

11. (Cancelled)

12. (Original) The system of claim 10 wherein said network processor determines a

memory channel for a memory access by determining whether said memory access is to an

interleaved portion of memory and if the access is to an interleaved portion then performing an

operation on said program address and when said program memory address does not access an

Applicants : Kuo et al.
Serial No. : 10751,263
Filed : December 30, 2003
Page : 6 of 14

Attorney's Docket No.: Intel-010PUS
Intel Docket No.: P17937

interleaved portion of memory then selecting the memory channel containing non-interleaved memory.

13. (Original) The system of claim 10 wherein said network processor maps said program address to a physical address by determining whether the program address accesses an interleaved portion of memory and when said program memory address does access the interleaved portion of memory then performing address interleaving of said program address and when said program memory address does not access the interleaved portion of memory then subtracting a predetermined value from said program address to obtain a physical address in the selected memory channel.

14. (Currently Amended) An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

assigning a first memory to a first memory channel;

assigning a second memory to a second memory channel; the first memory being equal in memory size to the second memory;

assigning a third memory to a third memory channel; the third memory comprising a first memory portion being equal in memory size to the first memory and comprising a second memory portion;

interleaving the first memory, the second memory and the first memory portion of

the third memory in a three-way interleaving;

allocating memory non-uniformly between a plurality of memory channels;

determining a selected memory channel from the first memory channel, the

second memory channel and the third memory channel said plurality of memory channels

for a program address; and

mapping said program address to a physical address within said selected memory

channel.

15. (Cancelled)

16. (Original) The article of claim 14 wherein said determining a selected memory

channel comprises:

determining whether the program address accesses an interleaved portion of memory and

when said program memory address does access an interleaved portion of memory then

performing an operation on said program address to obtain a memory channel number and when

said program memory address does not access an interleaved portion of memory then selecting

the memory channel containing non-interleaved memory.

17. (Original) The article of claim 14 wherein said mapping said program address to a

physical address comprises:

Applicants : Kuo et al.
Serial No. : 10751,263
Filed : December 30, 2003
Page : 8 of 14

Attorney's Docket No.: Intel-010PUS
Intel Docket No.: P17937

determining whether the program address accesses an interleaved portion of memory and when said program memory address does access the interleaved portion of memory then performing address interleaving of said program address and when said program memory address does not access the interleaved portion of memory then subtracting a predetermined value from said program address to obtain a physical address in the selected memory channel.

18. (Original) A method comprising:

designating a range of addresses defined as the memory between an upper address to perform range checking and a lower address to perform range checking;

monitoring memory accesses; and

determining if any of said memory accesses occur within said range of addresses and in response to a memory access occurring with said range of memory addresses then performing a predetermined operation.

19. (Original) The method of claim 18 wherein said performing a predetermined operation comprises performing an operation selected from the group consisting of interrupting the core processor, aborting the pending memory operation, executing a halt, and sending an exception.

20. (Original) The method of claim 18 wherein said determining if any of said memory accesses occur within said range of addresses comprises determining at least one of the group

Applicants : Kuo et al.
Serial No. : 10751,263
Filed : December 30, 2003
Page : 9 of 14

Attorney's Docket No.: Intel-010PUS
Intel Docket No.: P17937

consisting of determining if the starting address of the memory access lies between said upper address and said lower address, determining if the ending address of the memory access lies between said upper address and said lower address, and determining if the lower address lies between the starting address of the memory access and the ending address of the memory access.

21. (Original) The method of claim 18 wherein said upper address and said lower address are located in different blocks of memory.

22. (Original) The method of claim 18 wherein said starting address of a memory access and an ending address of the memory access are located in different blocks of memory.

23. (Original) An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

designating a range of addresses defined as the memory between an upper address to perform range checking and a lower address to perform range checking; and

monitoring memory accesses and determining if any of said memory accesses occur within said range of addresses and in response to a memory access occurring with said range of memory addresses then performing a predetermined operation.

Applicants : Kuo et al.
Serial No. : 10751,263
Filed : December 30, 2003
Page : 10 of 14

Attorney's Docket No.: Intel-010PUS
Intel Docket No.: P17937

24. (Original) The article of claim 23 wherein said performing a predetermined operation comprises performing an operation selected from the group consisting of interrupting the core processor, aborting the pending memory operation, executing a halt, and sending an exception.

25. (Original) The article of claim 23 wherein said determining if any of said memory accesses occur within said range of addresses comprises determining at least one of the group consisting of determining if the starting address of the memory access lies between said upper address and said lower address, determining if the ending address of the memory access lies between said upper address and said lower address, and determining if the lower address lies between the starting address of the memory access and the ending address of the memory access.

26. (Original) The article of claim 23 wherein said upper address and said lower address are located in different blocks of memory.

27. (Original) The article of claim 23 wherein said starting address of a memory access and an ending address of the memory access are located in different blocks of memory.